Abstract

A digital system and method of operation is provided in which several processors (400[]) are connected to a shared resource (432). Each processor has a translation lookaside buffer (TLB) (310[]) that contains recently used page entries that each includes an access priority value. Access priority values are assigned to regions of address space, typically pages, according to the program or data that is stored on a given page. Access priority values are maintained in page tables with address translations, such that when a translated page address is loaded into a TLB, the access priority associated with that page is included in the TLB page entry. Arbitration circuitry (430) is connected to receive a request signal from each processor along with an access priority value (353[]) from each TLB in response to the requested address. The arbitration circuitry is operable to schedule access to the shared resource according to the access priority values provided by the TLBs.